In the Claims:

1. (Currently Amended) An integrated circuit comprising:

an active termination circuit having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential, the second source potential being lower than the first source potential, the active termination circuit including at least one termination node being coupled to a common node between the first and second transistors; and

a control circuit operable to bias the first and second ~~transistor~~ transistors, wherein the control circuit includes a first control terminal control circuit operable to provide a first control terminal drive signal to a control terminal of the first transistor, and a second control terminal control circuit operable to provide a second control terminal drive signal to a control terminal of the second transistor, and wherein the first and second control terminal drive signals are such that a quiescent voltage potential of the common node is between the first source potential and the second source potential; and

wherein the first control terminal drive signal and the second control terminal drive signal are controlled such that a quiescent current conducted through the first and second transistors is substantially less than a current through two resistors whose parallel resistance approximates the characteristic impedance of a coupled transmission line.

2. (Original) The integrated circuit as in claim 1 wherein the control circuit is operable to bias the first and second transistors such that they provide a clamping function at the common node.

3. (Currently Amended) The integrated circuit of claim 1 wherein:

the first transistor is a MOSFET of the N-channel type and the second transistor is a MOSFET of the P-channel type;

the drain of the first MOSFET is coupled to the Vdd node, and the drain of the second MOSFET is coupled to the Vss node; and

[[the]] sources of both MOSFETs are coupled together and to the common node.

4. (Canceled)

5. (Currently Amended) The integrated circuit of ~~claim 4~~claim 1 wherein the quiescent voltage potential of the common node is at about a midpoint between the ~~Vdd and Vss~~ first and second source potentials.

6. (Currently Amended) The integrated circuit of claim [[4]] 33 wherein the first and second control terminal control circuits are operable to provide [[a]] the first control terminal drive signal to [[a]] the control terminal of the first transistor and [[a]] the second control terminal drive signal to [[a]] the control terminal of the second transistor to control the quiescent ~~switch~~ current through the first and second transistors.

7 - 9. (Canceled)

10. (Currently Amended) The integrated circuit of claim 1 and further comprising:

a third transistor having a current path and a control terminal, the current path coupled between the first transistor and the ~~voltage source~~ Vdd node; and

a fourth transistor, having a current path and a control terminal, the current path coupled between the second transistor and the ~~voltage source~~ Vss node wherein the operation of the first and second transistors can be selectively enabled or disabled by control signals coupled to the control terminals of the third and fourth transistors.

11. (Original) The integrated circuit of claim 10 wherein the third transistor is a P-channel MOSFET and the fourth transistor is an N-channel MOSFET.

12. (Currently Amended) ~~The~~ An integrated circuit of ~~claim 1~~ comprising:

an active termination circuit having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential, the second source potential being lower than the first source potential, the active termination circuit including at least one termination node being coupled to a common node between the first and second transistors;

a control circuit operable to bias the first and second transistor, wherein the control terminal control circuit ~~preferably~~ includes a fifth transistor and a sixth transistor coupled in series ~~across a~~ between the Vdd node ~~of a first source potential~~ and [[a]] the Vss node ~~of a second source potential~~ and scaled to the first and second transistors; and

a current source coupled to at least one of the fifth or sixth transistor, the current source controlling a ~~that controls the~~ quiescent current level in the first and second transistors.

13. (Original) The integrated circuit of claim 12 wherein the fifth transistor is an N-channel MOSFET, and the sixth transistor is a P-channel MOSFET.

14. (Currently Amended) The integrated circuit of claim 1 wherein the control circuit ~~preferably~~ includes a voltage source operable to produce a voltage potential of about a midpoint of the voltages of the ~~voltage sources Vdd and Vss~~ first source potential and the second source potential.

15. (Currently Amended) The integrated circuit of claim 1 wherein the control circuit ~~preferably~~ includes a voltage source operable to produce a voltage potential responsive to an externally supplied input voltage.

16. (Original) The integrated circuit of claim 1 and further comprising a resistor coupled between the common node and the termination node.

17. (Currently Amended) An active termination circuit, comprising:

a first MOSFET having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to a common node, and the drain terminal coupled to a Vdd node of a first source potential, wherein the first MOSFET comprises an n-channel MOSFET;

a second MOSFET having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to the common node, and the drain terminal coupled to a Vss node of a second source potential, the second source potential being lower than the first source potential, wherein the second MOSFET comprises a p-channel MOSFET; and

a control circuit operable to bias the first and second MOSFETs;

wherein the gate terminal of the first MOSFET is coupled to a voltage source between the first and second source potentials and the gate terminal of the second MOSFET is coupled to

another voltage source of a lower potential and wherein the potential difference between the voltage sources coupled to the gates of the first and second MOSFETs is controlled by a current source.

18. (Currently Amended) The active termination circuit of claim 17 wherein the control circuit operates to bias the first and second MOSFETs such that ~~they exhibit~~ a controlled impedance is exhibited at the common node.

19-21. (Canceled)

22. (Original) The active termination circuit of claim 17 wherein the control circuit comprises:

a first operational amplifier with an output coupled to the gate terminal of the first MOSFET; and

a second operation amplifier with an output coupled to the gate terminal of the second MOSFET.

23. (Currently Amended) ~~The~~ An active termination circuit ~~of claim 22, comprising~~:

a first MOSFET having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to a common node, and the drain terminal coupled to a Vdd node of a first source potential, wherein the first MOSFET is an N-channel MOSFET;

a second MOSFET having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to the common node, and the drain terminal coupled to a Vss

node of a second source potential, the second source potential being lower than the first source potential, wherein ~~and~~ the second MOSFET is a P-channel MOSFET; and

a control circuit operable to bias the first and second MOSFETs, wherein the control circuit comprises a first operational amplifier with an output coupled to the gate terminal of the first MOSFET and a second operation amplifier with an output coupled to the gate terminal of the second MOSFET;

wherein the first operational amplifier is powered by a power supply potential greater than [[Vdd]] the first source potential and the second operational amplifier is powered by a power supply potential less than [[Vss]] the second source potential, the first and second operational amplifiers capable of producing gate drive signals greater than the ~~power supply~~ first source potential [[Vdd]] and less than the ~~power supply~~ second source potential [[Vss]], respectively.

24. (Currently Amended) The active termination circuit of claim 23 and further comprising:

a third MOSFET with a channel coupled between the Vdd node and the first operational amplifier, the third MOSFET having a gate terminal coupled to the gate terminal of the first MOSFET, the third MOSFET being an N-channel MOSFET; and

a fourth MOSFET with a channel coupled between the Vss node and the [[first]] second operational amplifier, the fourth MOSFET having a gate terminal coupled to the gate terminal of the second MOSFET, the fourth MOSFET being a P-channel MOSFET.

25. (Currently Amended) The active termination circuit of claim 17 and further comprising a first enable switch coupled between the first MOSFET and the Vdd node and a second enable switch coupled between the second MOSFET and the Vss node.

26. (Canceled)

27. (Currently Amended) A method of operating an active termination circuit, the method comprising:

biasing first and second series coupled transistors of opposite type such that they exhibit a controlled impedance at a common node thereof, wherein the first and second transistors are coupled in series ~~aeress~~ between a Vdd node of a first source potential and a Vss node of a second source potential, the common node being between the first and second transistors, and the second source potential being lower than the first source potential;

wherein device geometries, device size, and processing of the first and second transistors are scaled so that a controlled impedance and a quiescent voltage potential are generated at the common node in response to induced voltages produced by a driver circuit that couples communication signals to the common node.

28. (Currently Amended) The method of claim 27 wherein biasing first and second series coupled transistors comprises producing first and second control terminal drive signals and applying said first and second control terminal drive ~~signal~~ signals to the first and second series coupled transistors, the first and second control terminal drive signals produced such that the

quiescent voltage potential of the common node is between the [[Vdd]] first source and [[Vss]] second source potentials.

29. (Original) The method of claim 28 wherein the first and second series coupled transistors are MOSFETs.

30. (Currently Amended) The method of claim 27 wherein the quiescent voltage potential of the common node is produced at about a midpoint between the [[Vdd]] first source potential and [[Vss]] second source potential[[s]].

31. (Canceled)

32. (New) An integrated circuit comprising:

an active termination circuit having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential, the second source potential being lower than the first source potential, the active termination circuit including at least one termination node that is coupled to a common node between the first and second transistors; and

a control circuit operable to bias the first and second transistors, wherein the control circuit includes a first control terminal control circuit operable to provide a first control terminal drive signal to a control terminal of the first transistor, and a second control terminal control circuit operable to provide a second control terminal drive signal to a control terminal of the second transistor, wherein the first and second control terminal drive

signals are such that a quiescent voltage potential of the common node is between the Vdd and Vss potentials; and

wherein device geometries, device size, and processing of the first and second transistors are scaled so that they achieve a controlled impedance and the quiescent voltage potential at the common node in response to an induced voltages produced by a driver circuit that couples communication signals to the termination node, and wherein the quiescent voltage potential is at about a midpoint between the first source potential and the second source potential.

33. (New) An integrated circuit comprising:

an active termination circuit having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential, the second source potential being lower than the first source potential, the active termination circuit including at least one termination node that is coupled to a common node between the first and second transistors; and

a control circuit operable to bias the first and second transistors, wherein the control circuit includes a first control terminal control circuit operable to provide a first control terminal drive signal to a control terminal of the first transistor, and a second control terminal control circuit operable to provide a second control terminal drive signal to a control terminal of the second transistor, wherein the first and second control terminal drive signals are such that a quiescent voltage potential of the common node is between the Vdd and Vss potentials; and

wherein the first and second control terminal control circuits are operable from voltage

sources that are greater than the first source potential for the first control terminal control circuit, and less than the second source potential for the second control terminal control circuit, and are capable of providing control terminal control signals, respectively, that are greater than the first source potential and less than the second source potential.